What is claimed is:

1. An electrically programmable three-dimensional integrated memory (EP-3DiM), comprising:

a substrate circuit, said substrate circuit further comprising a substrate integrated circuit and an address-decoder, said substrate integrated circuit comprising an embedded RWM and/or an embedded processor;

at least an electrically programmable three-dimensional memory (EP-3DM) level, said EP-3DM level being stacked on top of said substrate circuit and connected with said substrate circuit through a plurality of inter-level connecting vias, said address-decoder decoding address for at least a portion of said EP-3DM level.

2. The EP-3DiM according to claim 1, wherein

said embedded RWM comprises an embedded RAM, at least a portion of the input/output of said embedded RAM being eventually connected with at least a portion of the input/output of said address-decoder, whereby said embedded RAM stores a copy of the data from said EP-3DM.

3. The EP-3DiM according to claim 1, wherein

said embedded RWM comprises an embedded ROM, whereby said embedded ROM stores correctional data for said EP-3DM level; and

said substrate circuit further comprises means for selecting data from said EP-3DM level or from said embedded ROM.

4. The EP-3DiM according to claim 1, wherein

said embedded RWM comprises an embedded ROM, whereby said embedded ROM stores upgrade codes for said EP-3DM level; and

said substrate circuit further comprises means for selecting data from said EP-3DM level or from said embedded ROM.

5. The EP-3DiM according to claim 1, wherein

at least a portion of said embedded RWM and at least a portion of said EP-3DM form a unified memory space; and

said substrate circuit further comprises an address-translation block and an address-decoder for said unified memory space, at least a portion of the output of said address-translation block being eventually connected with at least a portion of the input of said address-decoder for said unified memory space.

6. The EP-3DiM according to claim 1, wherein

said embedded processor is selected from a group consisting of D/A converter, decoder and decryption engine.

7. An electrically programmable three-dimensional memory (EP-3DM), comprising:

a substrate circuit, said substrate circuit comprising a plurality of active devices and an interconnect system connecting said active devices, said substrate circuit further comprising an address-decoder;

at least an EP-3DM level stacked on top of said substrate circuit and connected with said substrate circuit through a plurality of inter-level connecting vias, said EP-3DM level comprising a plurality of address-selection lines and EP-3DM cells, said address-decoder decoding address for at least a portion of said EP-3DM level.

8. The EP-3DM according to claim 7, wherein

said address-selection lines in said EP-3DM level comprises poly-crystalline semiconductor materials; and

said interconnect system of said substrate circuit is made of refractory conductor and thermally-stable dielectric.

9. The EP-3DM according to claim 7, further comprising a shielding layer between said substrate circuit and at least a portion of said EP-3DM level.

10. The EP-3DM according to claim 7, further comprising:

at least an interconnect gap between two adjacent address-selection lines on said EP-3DM level;

at least an embedded wire, said embedded wire passing through said EP-3DM level in said interconnect gap.

11. The EP-3DM according to claim 7, further comprising at least a routing level in said interconnect system of said substrate circuit, said routing level providing electrical connection between said EP-3DM level and said substrate circuit, whereby at least a portion of said address-decoder is located under said EP-3DM level.

12. The EP-3DM according to claim 7, wherein

at least an address-selection line in said EP-3DM level is a composite line, said composite line comprising a highly-conductive layer and a lightly-doped layer, said lightly-doped layer being located at the bottom of said composite line; and

said EP-3DM further comprises a via and an inverted-U link, said via being located near one end of said composite line and said inverted-U link having an inverted-U shape, said via being connected with said composite line through said inverted-U link by making contacts to said highly-conductive layer on top and/or on sidewalls.

13. An electrically programmable three-dimensional memory (EP-3DM) cell, comprising:

a first top electrode;

a second bottom electrode;

a 3D-ROM layer between said first and second electrodes, said 3D-ROM layer further comprising an antifuse layer, said antifuse layer having a high resistance when un-programmed and a low resistance when programmed.

14. The EP-3DM cell according to claim 13, wherein said 3D-ROM layer comprises semiconductor materials with large bandgap.

15. The EP-3DM cell according to claim 13, wherein

at least one of said first and second electrodes further comprises a semiconductor layer and a metallic layer, said semiconductor layer comprising doped semiconductor materials and said metallic layer comprising metallic materials.

16. The EP-3DM cell according to claim 13, wherein at least one of said first and second electrodes further comprises a semiconductor layer, said semiconductor layer being doped by metallic ions.

17. The EP-3DM cell according to claim 13, wherein said 3D-ROM layer is a polarized layer.

18. The EP-3DM cell according to claim 13, wherein said EP-3DM cell has a polarized structure.

19. The EP-3DM cell according to claim 13, wherein said 3D-ROM layer comprises micro-crystalline semiconductor materials.

20. The EP-3DM cell according to claim 13, wherein said EP-3DM cell is a seamless cell or a quasi-seamless cell.